Appendix

The amplitude, output current, and phase jitter* of differential outputs are shown in Figures 1 and 2. LVDS, LV-PECL, and HCSL are depicted in red. WA-LVDS is blue.

Figure 1
The difference between the H and L levels, which correspond to amplitude, is defined as 0.35 V for LVDS. While the output current is small, the amplitude is low, resulting in LVDS having inferior noise immunity compared to that of LV-PECL and HCSL. On the other hand, LV-PECL and HCSL have large amplitudes but consume a large amount of current. WA-LVDS amplitude is selectable in small increments, from the same level as LVDS to the levels corresponding to LV-PECL and HCSL. Moreover, WA-LVDS output current is kept low, contributing to low current consumption.

Figure 2
As WA-LVDS amplitude increases, phase jitter decreases, resulting in differential output with low noise.

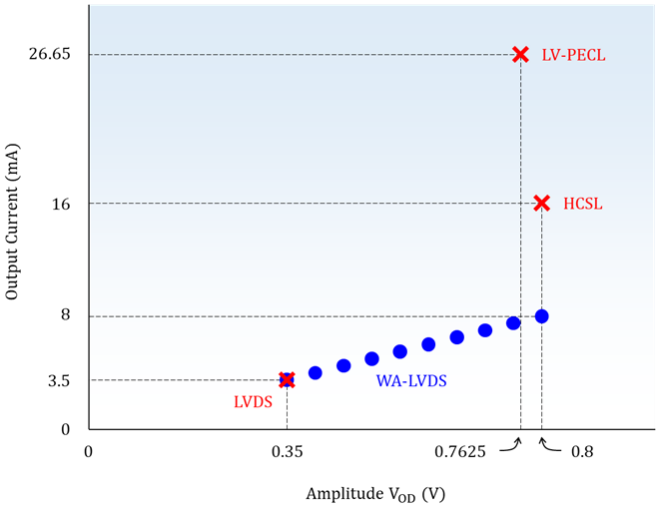

Figure 1: Amplitude vs. output current for differential

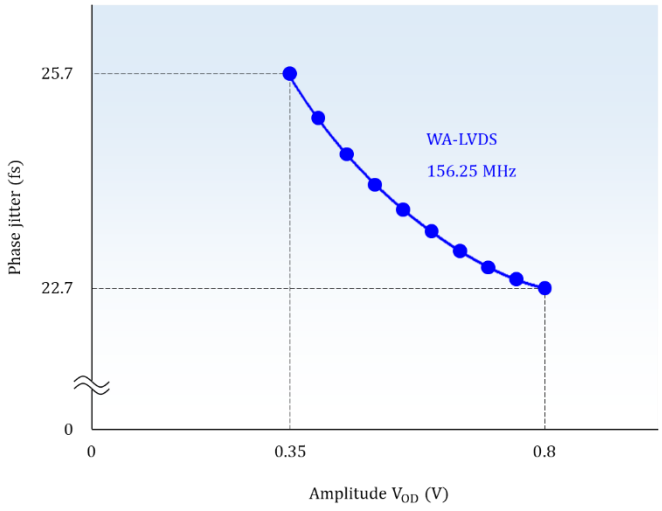

Figure 2: WA-LVDS phase jitter

*: Phase jitter: Fluctuation of the clock period is called jitter. Phase jitter is a measure of edge deviation from a jitter-free ideal clock and can be calculated from the phase noise characteristic.